CLAIMS

We claim:

1. A method for monitoring the occurrences of one or more events related to the operation of a processor, said processor including a performance monitor having a plurality of counting elements, said method comprising the steps of:

identifying the number of events to be counted by said performance monitor;

identifying the number of counting elements available to count incidences of said events; and

assigning at least two of said counting elements to serially count incidences of at least one of said events.

2. A method as set forth in claim 1, wherein said performance monitor further includes at least one control element, said control element performing said steps of identifying the number of events, identifying the number of counting elements, and assigning of said counting elements.

3. A method as set forth in claim 2, wherein said assigning step comprises at least the steps of:

dividing the number of available counting elements by the number of events to be counted;

assigning a number of counting elements, equal to the integer resulting from said dividing step, to each of said events to be counted; and

assigning one additional counting element, equal in number to any remainder left over from said dividing step, to as many of said events to be counted as possible.

4. A method as set forth in claim 2, wherein said assigning step comprises at least the steps of:

determining the historical frequency of occurrence of incidences of said events to be counted; and

assigning said available counters to said events to be counted based upon said determined historical frequency.

5. A method as set forth in claim 2,, wherein said counting elements each comprise a performance monitor counter, and wherein each control element comprises a monitor mode control register.

6. A performance monitor for monitoring the occurrence of incidences of one or more events related to the operation of a processor, comprising:

at least one monitor mode control register; and

a plurality of performance monitor counters operatively connected to said monitor mode control register, said monitor mode control register grouping said performance

monitor counters so that when one of said performance monitor counters reaches capacity in connection with the counting incidences of a first of said events, a second of said performance monitor counters begins counting subsequent incidences of said first of said events.

7. A performance monitor for monitoring the occurrence of incidences of one or more events related to the operation of a processor, comprising:

at least one control element; and

a plurality of counting elements operatively coupled to said control element, said control element grouping said counting elements so that when one of said counting elements reaches capacity in connection with the counting of incidences of a first of said events, a second of said counting elements begins counting subsequent incidences of said first of said events.

8. A computer program product in a computer-readable medium for monitoring the occurrences of one or more events related to the operation of a processor, said processor including a performance monitor having a plurality of counting elements, said computer program product comprising:

first instructions for identifying the number of events to be counted by said performance monitor;

second instructions for identifying the number of counting elements available to count incidences of said events; and

third instructions for assigning at least two of said counting elements to serially count incidences of at least one of said events.

9. A computer program product as set forth in claim 8, wherein said performance monitor further includes at least one control element, said control element providing said first, second, and third instructions.

10. A computer program product as set forth in claim 9, wherein said third instructions include at least:

fourth instructions for dividing the number of available counting elements by the number of events to be counted;

fifth instructions for assigning a number of counting elements, equal to the integer resulting from the execution of said fourth instructions, to each of said events to be counted; and

sixth instructions for assigning one additional counting element, equal in number to any remainder left over from execution of said fourth instructions, to as many of said events to be counted as possible.

11. A computer program product as set forth in claim 9, wherein said third instructions comprise at least:

fourth instructions for determining the historical frequency of occurrence of incidences of said events to be counted; and

fifth instructions for assigning said available counters to said events to be counted based upon said determined historical frequency.

12. A computer program product as set forth in claim 9, wherein said counting elements each comprise a performance monitor counter, and wherein each control element comprises a monitor mode control register.

13. A system for monitoring the occurrences of one or more events related to the operation of a processor, said processor including a performance monitor having a plurality of counting elements, said system comprising:

means for identifying the number of events to be counted by said performance monitor;

means for identifying the number of counting elements available to count incidences of said events; and

means for assigning at least two of said counting elements to serially count incidences of at least one of said events.

14. A system as set forth in claim 13, wherein said performance monitor further includes at least one control element, said control element identifying the number of events, identifying the number of counting elements, and assigning of said counting elements.

15. A system as set forth in claim 13, wherein said assigning step comprises at least:

means for dividing the number of available counting elements by the number of events to be counted;

means for assigning a number of counting elements, equal to the integer resulting from the division performed by said dividing means, to each of said events to be counted; and

means for assigning one additional counting element, equal in number to any remainder left over from said division performed by said dividing , to as many of said events to be counted as possible.

16. A system as set forth in claim 13, wherein said assigning means comprises at least:

means for determining the historical frequency of occurrence of incidences of said events to be counted; and

means for assigning said available counters to said events to be counted based upon said determined historical frequency.

17. A system as set forth in claim 13, wherein said counting elements each comprise a performance monitor counter, and wherein each control element comprises a monitor mode control register.